DETAILED ACTION

The previous final Office Action has been vacated and is replaced by this instant Final Office Action in view of the previous amendments dated July 24, 2008.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claims 1-2, 4-6, 10, 12, 25, 27-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kumar (US 2004/0028040) in view of Shadmon (US 2003/0204515) and Rangarajan (US 2004/0008634).

Regarding claim 1, Kumar describes a method, comprising:

receiving a packet at a network device, the packet including a destination address (para. 22);

indexing into a table using a portion of the destination address to locate an entry in the table associated with the portion of the destination address (para. 32, indexing a trie data structure 500 (table) entry using device address prefix);

deriving an index associated with the portion of the destination address to identify the trie structure in a same memory unit (para. 31, index to trie structure is associated with first eight bits of destination address, the (all) information being stored in memory 240, para. 28 & 32).

navigating the entry and the pool of data blocks that is identified to find a next-hop for the packet (para. 33, trie data structure 500 and associated information 600 is used to determine the route pointer 602).

Kumar fails to explicitly describe that the trie structure to be indexed comprises a pool of trie blocks, and indexing among a plurality of pools of trie blocks.

Shadmon describes: a trie comprising a plurality of trie blocks to be indexed (fig. 7 & para. 3, an index for a balanced structure of trie blocks).

It would have been obvious to one with ordinary skill in the art at the time of invention by applicant to specify that the trie structure of Kumar comprises a pool of trie blocks to be indexed as in Shadmon.

The motivation for combining the teachings is that it allows for the maintenance of a balanced trie structure of blocks (Shadmon, para. 70).

Kumar and Shadmon combined describe that each trie block comprises a plurality of trie entries (fig. 7 & para. 48, trie lookup blocks each comprising a plurality of nodes (entries)), but fails to explicitly describe:

each trie entry comprising a next hop pointer and a next trie pointer to reference trie entries located in the pool of trie blocks including the next-hop pointer and next-trie pointer.

Rangaranjan suggests as a common art that: each trie entry comprising a next hop pointer and a next trie pointer to reference trie entries located in the pool of trie blocks including the next-hop pointer and the next-trie pointer (para. 8, each trie node

(entry) comprises a next hop pointer & a pointer to the block of child nodes (next trie entries in the pool of trie blocks including the next-hop pointer and the next-trie pointer)).

It would have been obvious to one with ordinary skill in the art at the time of invention by applicant to specify the details of the trie entry mention above as in Rangaranjan for the trie entries of Kumar and Shadmon combined.

The motivation for combining the teachings is that it allows the achievement of network & systems which performs communication at a greater speed and capacity (Rangaranjan, para. 2).

Regarding claim 10, Kumar describes a method, comprising:

receiving a packet at a router, the packet including a destination internet protocol (IP) address (para. 22);

indexing into a table comprising a plurality of trie entries using a portion if the destination IP address to find a trie entry of the plurality of trie entries (para. 30-31, indexing trie table's entries using the destination address's prefix bits), wherein each trie entry comprises 64-bits (para. 64-65, trie entry has 64 bits to compares with the IPv6's 64 bits destination address);

deriving an index associated with the portion of the destination address to identify the trie structure in a same memory unit (para. 31, index to trie structure is associated with first eight bits of destination address, the (all) information being stored in memory 240, para. 28 & 32).

navigating the trie entry and the pool of trie blocks that is identified to follow the trie entry to find a next-hop for the packet (para. 32-33, trie lookup algorithm determines the transmitted next hop).

Kumar fails to explicitly describe that the trie structure to be indexed comprises a pool of trie blocks, and indexing among a plurality of pools of trie blocks.

Shadmon describes: a trie comprising a plurality of trie blocks to be indexed (fig. 7 & para. 3, an index for a balanced structure of trie blocks).

It would have been obvious to one with ordinary skill in the art at the time of invention by applicant to specify that the trie structure of Kumar comprises a pool of trie blocks to be indexed as in Shadmon.

The motivation for combining the teachings is that it allows for the maintenance of a balanced trie structure of blocks (Shadmon, para. 70).

Kumar and Shadmon combined describe that each trie block comprises a plurality of trie entries (fig. 7 & para. 48, trie lookup blocks each comprising a plurality of nodes (entries)), but fails to explicitly describe:

each trie entry comprising a next hop pointer and a next trie pointer to reference trie entries located in the pool of trie blocks including the next-hop pointer and next-trie pointer.

Rangaranjan suggests as a common art that: each trie entry comprising a next hop pointer and a next trie pointer to reference trie entries located in the pool of trie blocks including the next-hop pointer and the next-trie pointer (para. 8, each trie node

(entry) comprises a next hop pointer & a pointer to the block of child nodes (next trie entries in the pool of trie blocks including the next-hop pointer and the next-trie pointer)).

It would have been obvious to one with ordinary skill in the art at the time of invention by applicant to specify the details of the trie entry mention above as in Rangaranjan for the trie entries of Kumar and Shadmon combined.

The motivation for combining the teachings is that it allows the achievement of network & systems which performs communication at a greater speed and capacity (Rangaranjan, para. 2).

Regarding claim 25, Kumar describes a network device, comprising:

a plurality of ports (fig. 1, network device 120 has ports to end devices 122);

a processor communicatively coupled to each of the plurality of ports (fig. 2, controller (processor) within the network device 200);

a storage device operatively coupled to the processor (fig. 2, local cache 232 & memory unit 240), the storage device including a plurality of instructions which when executed by the processor perform operations comprising:

receiving a packet at a first port of the plurality of ports, the packet including a destination address (para. 22);

indexing into a table using a portion of the destination address to locate an entry in the table associated with the portion of the destination address (para. 32, indexing a trie data structure 500 (table) entry using device address prefix);

deriving an index associated with the portion of the destination address to identify the trie structure in a same memory unit (para. 31, index to trie structure is associated

with first eight bits of destination address, the (all) information being stored in memory 240, para. 28 & 32).

navigating the entry and the pool of trie blocks to find a next-hop for the packet (para. 33, trie data structure 500 and associated information 600 is used to determine the route pointer 602);

outputting the packet from a second port of the plurality of ports to the next-hop (para. 13, network device 120 output packet to the port directed to the respective destination device 132).

Kumar fails to explicitly describe that the trie structure to be indexed comprises a pool of trie blocks, and indexing among a plurality of pools of trie blocks.

Shadmon describes: a trie comprising a plurality of trie blocks to be indexed (fig. 7 & para. 3, an index for a balanced structure of trie blocks).

It would have been obvious to one with ordinary skill in the art at the time of invention by applicant to specify that the trie structure of Kumar comprises a pool of trie blocks to be indexed as in Shadmon.

The motivation for combining the teachings is that it allows for the maintenance of a balanced trie structure of blocks (Shadmon, para. 70).

Kumar and Shadmon combined describe that each trie block comprises a plurality of trie entries (fig. 7 & para. 48, trie lookup blocks each comprising a plurality of nodes (entries)), but fails to explicitly describe:

each trie entry comprising a next hop pointer and a next trie pointer to reference trie entries located in the pool of trie blocks including the next-hop pointer and next-trie pointer.

Rangaranjan suggests as a common art that: each trie entry comprising a next hop pointer and a next trie pointer to reference trie entries located in the pool of trie blocks including the next-hop pointer and the next-trie pointer (para. 8, each trie node (entry) comprises a next hop pointer & a pointer to the block of child nodes (next trie entries in the pool of trie blocks including the next-hop pointer and the next-trie pointer)).

It would have been obvious to one with ordinary skill in the art at the time of invention by applicant to specify the details of the trie entry mention above as in Rangaranjan for the trie entries of Kumar and Shadmon combined.

The motivation for combining the teachings is that it allows the achievement of network & systems which performs communication at a greater speed and capacity (Rangaranjan, para. 2).

Regarding claim 2, Kumar further describes that an entry in the table comprises a next-hop pointer and a next-trie pointer (fig. 6, entry comprising route pointer & next trie pointer).

Regarding claims 4 and 12, Kumar further describes:

navigating the entry and the pool of trie blocks comprises: updating a next-hop-to-return with the next-hop pointer if the next-hop pointer is not null (para. 33, updating current router pointer (next-hop-to-return) if extracted route pointer 602 is not null);

following the next-trie pointer to a trie block within the pool if the next-trie pointer is not null and indexing into the trie block with a second portion of the destination address (fig. 5 & para. 34, indexing subsequent non-null trie tree entries using different destination address prefix bits); and following the next-hop-to-return to a next-hop table if the next-trie pointer is null (para. 32, current router pointer (next-hop-to-return) remains unchanged if next-trie pointer is null).

Regarding claims 5 and 27, Kumar further describes: deriving the pool index comprises performing a hash on the portion of the destination address to obtain the pool index (para. 19, use hashing to perform the search, fig. 2, hashing unit).

Regarding claim 6, Kumar, Shadmon and Rangarajan combined and further suggest:

deriving the pool index comprises reading the pool index associated with the portion of the destination address from the entry in the table (Kumar, para. 31, index stored at memory (entry in table) is a portion of the destination address), wherein the pool index is a separate field in addition to a next-hop pointer and next-trie pointer in the entry in the table (Rangarajan, para. 8, next-hop pointer and next-trie pointer are independent items (additional fields) in a trie node (entry)).

Regarding claim 28, Kumar further suggests: deriving the pool index comprises reading the pool index associated with the portion of the destination address from the entry in the table (para. 31-32, reading latter prefix bits associated with the destination address at the point when third table entry is addressed, see fig. 5).

2. Claims 7 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kumar in view of Shadmon and Rangarajan, and further in view of Du (US 5,694,591).

Regarding claim 7, Kumar, Shadmon and Rangarajan combined describe a trie structure (table) where each entry is indexed by a portion of a particular destination address, but fails to describe:

examining the plurality of pools of trie blocks to find an under-utilized pool;

adding a second entry to the table indexed by a portion of a second destination address, a second pool index associated with the portion of the second destination address to correspond to the under-utilized pool.

Du describes a tree balancing method comprising:

examining the plurality of pools of trie blocks to find an under-utilized pool (col. 8, lines 53-67, comparing the deep-left (potential overflow pool) branching costs in balancing a tree from fig. 1 to fig. 2);

adding a second entry to the table a second pool index to correspond to the under-utilized pool (col. 8, lines 1-9, ship/relocate tuples (add entries with indices to the right-branching (under-utilized pool) in transforming the data structure into a "balanced bushy tree")).

It would have been obvious to one with ordinary skill in the art at the time of invention by applicant to utilize the scheme of Du to resolve imbalance tree structures (with under-utilized pool) for the tree structure stored for routing purposes of Kumar, Shadmon and Rangarajan combined.

The motivation for combining the teachings is that costs may be equalized within the search tree, resulting an optimal query response time (Du, col. 5, lines 14-19 & 25-31).

Regarding claim 9, Kumar, Shadmon and Rangarajan combined describe a trie structure (table) where each entry is indexed by a portion of a particular destination address, but fails to describe:

examining the plurality of pools of trie blocks to find a potential overflow pool;

adding a second entry to the table indexed by a portion of a second destination address, a second pool index associated with the portion of the second destination address not to be associated with the potential overflow pool.

Du describes:

examining the plurality of pools of trie blocks to find a potential overflow pool (col. 8, lines 53-67, comparing the deep-left (potential overflow pool) branching costs in balancing a tree from fig. 1 to fig. 2);

adding a second entry to the table indexed by a portion of a second destination address, a second pool index associated with the portion of the second destination address not to be associated with the potential overflow pool (col. 8, lines 1-9, ship/relocate tuples (add entries with indices to the right-branching (not associated with the potential overflow pool) in transforming the data structure into a "balanced bushy tree")).

It would have been obvious to one with ordinary skill in the art at the time of invention by applicant to utilize the above steps of Du to resolve the potential overflow in using the trie structure of Kumar, Shadmon and Rangarajan combined.

The motivation for combining the teachings is that costs may be equalized within the search tree, resulting an optimal query response time (Du, col. 5, lines 14-19 & 25-31).

3. Claims 13-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kumar in view of Shadmon, Rangaranjan, and Mathew (US 2004/0006639).

Regarding claim 13, Kumar describes a method, comprising:

receiving a packet at a network device, the packet including a destination internet protocol (IP) address (para. 22-23, IPv6 packet with destination address);

indexing into a table comprising a plurality of trie entries using a portion of the destination address to find an entry of the plurality of trie entries (para. 32, indexing into trie data structure 500 (table) using device address prefix), wherein each trie entry in the table comprises a next-hop pointer and a next-trie pointer (para. 33, trie data structure 500 and associated information 600 is used to determine the route pointer 602).

deriving an index associated with the portion of the destination address to identify the trie structure in a same memory unit (para. 31, index to trie structure is associated with first eight bits of destination address, the (all) information being stored in memory 240, para. 28 & 32).

navigating the entry and the pool of trie blocks that is identified to find a next-hop for the packet (para. 33, trie data structure 500 and associated information 600 is used to determine the route pointer 602 to route packet);

Kumar fails to explicitly describe that the trie structure to be indexed comprises a pool of trie blocks, and indexing among a plurality of pools of trie blocks.

Shadmon describes: a trie comprising a plurality of trie blocks to be indexed (fig. 7 & para. 3, an index for a balanced structure of trie blocks).

It would have been obvious to one with ordinary skill in the art at the time of invention by applicant to specify that the trie structure of Kumar comprises a pool of trie blocks to be indexed as in Shadmon.

The motivation for combining the teachings is that it allows for the maintenance of a balanced trie structure of blocks (Shadmon, para. 70).

Kumar and Shadmon combined describe that each trie block comprises a plurality of trie entries (fig. 7 & para. 48, trie lookup blocks each comprising a plurality of nodes (entries)), but fails to explicitly describe:

each trie entry comprising a next hop pointer and a next trie pointer to reference trie entries located in the pool of trie blocks including the next-hop pointer and next-trie pointer.

Rangaranjan suggests as a common art that: each trie entry comprising a next hop pointer and a next trie pointer to reference trie entries located in the pool of trie blocks including the next-hop pointer and the next-trie pointer (para. 8, each trie node

(entry) comprises a next hop pointer & a pointer to the block of child nodes (next trie entries in the pool of trie blocks including the next-hop pointer and the next-trie pointer)).

It would have been obvious to one with ordinary skill in the art at the time of invention by applicant to specify the details of the trie entry mention above as in Rangaranjan for the trie entries of Kumar and Shadmon combined.

The motivation for combining the teachings is that it allows the achievement of network & systems which performs communication at a greater speed and capacity (Rangaranjan, para. 2).

Kumar also describes route (next-hop) pointer and next trie pointer (fig. 6), but fails to explicitly describe: the next-trie pointer comprising more bits than the next-hop pointer.

Mathew describes: the next-trie pointer comprising more bits than the next-hop pointer (fig. 7 & para. 39, next trie is a 16-bit pointer whereas the next hop is a 15 bit pointer).

It would have been obvious to one with ordinary skill in the art at the time of invention by applicant to specify that the next trie pointer comprises more bits than the next-hop pointer as in Mathew for the trie entries in Kumar, Shadmon and Rangaranjan combined.

The motivation for combining the teachings is that it reduces the search and update times for routing information that may result in a faster processing of packets (Mathew, para. 1)

Regarding claim 14, Kumar Shadmon, Rangaranjan and Mathew combined describes:

the next-hop pointer comprises 8-bits and the next-trie pointer comprises 24-bits (Mathew, para. 39, variations of 32 bits total may comprise 8-bit next hop and 24-bit next-trie).

Claim 16 is an article of manufacture comprising the method as described in claim 1. Hence, it is rejected under the same rationale.

Claims 17, 19-22 and 24 are dependent claims comprising limitations described in claims 2, 4-7 and 9 respectively. Hence, it is rejected under the same rationale.

4. **Claim 26** is rejected under 35 U.S.C. 103(a) as being unpatentable over Kumar in view of Shadmon and Rangaranjan as applied to claim 25 above, and further in view of Choe (US 2002/0118682).

Kumar describes a plurality of pools of trie blocks (fig. 5, subset of trie search branches), but fails to describe:

the trie blocks are stored as a link list in a memory device operatively coupled to the processor (para. 51 & 55, the trie lookup structure in a linked list format).

It would have been obvious to one with ordinary skill in the art at the time of invention by applicant to use a linked list format for storing trie lookups as in Choe for the system of Kumar.

The motivation for combining the teachings is that it provides a method for performing high-speed IP route lookups and managing routing/forwarding tables (Choe, para. 17).

Allowable Subject Matter

5. **Claim 8** is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

6. Applicant's arguments with respect to claims 1, 2, 4-10, 12-14 and 25-28 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure: Sample (US 2005/0027679) describing method for ternary patricia trie blocks, Pin (US 2003/0198234) describing method for constructing and searching IP address, Liao (US 6,691,171) describing method for address lookup in data communications, and Jennings (US 6,804,230) describing communication device with forwarding database having a trie search facility.

Applicant's previous amendment dated July 24, 2008 necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS**

MADE FINAL. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to WARNER WONG whose telephone number is (571)272-8197. The examiner can normally be reached on 6:30AM - 3:00PM, M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kwang Yao can be reached on 571-272-3182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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